**CT 765 04**

**Course Objectives:**  
The main objective of the advanced computer aarchitecture is to provide advanced knowledge of computer architecture including parallel architectures, instruction-level parallel architectures, superscalar architectures, thread and process-level parallel architecture.

1. **Computational Models(6 hours)**
   1. computational model,
   2. the von Neumann Computational model,
   3. Evolution and interpretation of the concept of computer architecture,
   4. Interpretation of the concept of the computer architectures at different levels of abstraction,
   5. Multilevel hierarchical framework

1. **Parallel Processing(7 hours)**
   1. Process, Thread, Processes and threads in languages,
   2. Concurrent and parallel execution and programming languages,
   3. Types of available parallelism,
   4. Levels of available functional parallelism,
   5. Utilization of functional parallelism,
   6. Classification of parallel architectures,
   7. Relationships between languages and parallel architectures

1. **Pipelined Processors(7 hours)**
   1. Principle of pipelining,
   2. Structure of pipelines,
   3. Performance measures,
   4. Application scenarios of pipelines,
   5. Layout of a pipeline, Dependence resolution,
   6. Design space,
   7. Pipelined processing of loads and stores

1. **Superscalar Processors(8 hours)**
   1. The emergence and widespread adaption of superscalar processors,
   2. Specific tasks of superscalar processing,
   3. Parallel decoding,
   4. superscalar instruction issue,
   5. Scope of shelving,
   6. Layout of shelving buffers,
   7. Operand fetch policies,
   8. Instruction dispatch schemes ,
   9. Scope of register renaming with example

1. **Processing of control transfer Instructions(7 hours)**
   1. Types of branches,  Performance measures of branch processing ,
   2. branch handling ,
   3. Delayed branching,
   4. Branch processing,
   5. Multiday branching

1. **Thread and Process-level Parallel Architectures(10 hours)**
   1. MIMD architectures
   2. Distributed memory MIMD architectures,
   3. Fine-gain and  Medium-gain systems,
   4. Coarse-grain multicomputer,
   5. Cache coherence
   6. Uniform memory access(UMA) machines,
   7. Cache-coherent non-uniform memory access(CC-NUMA) machines,
   8. Cache only memory architecture(COMA)

**References:**

1. Advanced Computer Architectures: a design space approach, Deszo Sima, Terence Fountain, Peter Kacsuk
2. Computer Architecture and organization, John P. Hayes
3. Computer Organization and Design, David A. Patterson, John L. Hennessy

**Evaluation Scheme**:  
The questions will cover all the chapters of the syllabus. The evaluation scheme will be as indicated in the table below:

|  |  |  |
| --- | --- | --- |
| **Chapters** | **Hours** | **Marks Distribution\*** |
| 1 | 6 | 10 |
| 2 | 7 | 13 |
| 3 | 7 | 13 |
| 4 | 8 | 14 |
| 5 | 7 | 13 |
| 6 | 10 | 17 |
| **Total** | **45** | **80** |

\*There could be a minor deviation in Marks distribution